

FIG. 1 A

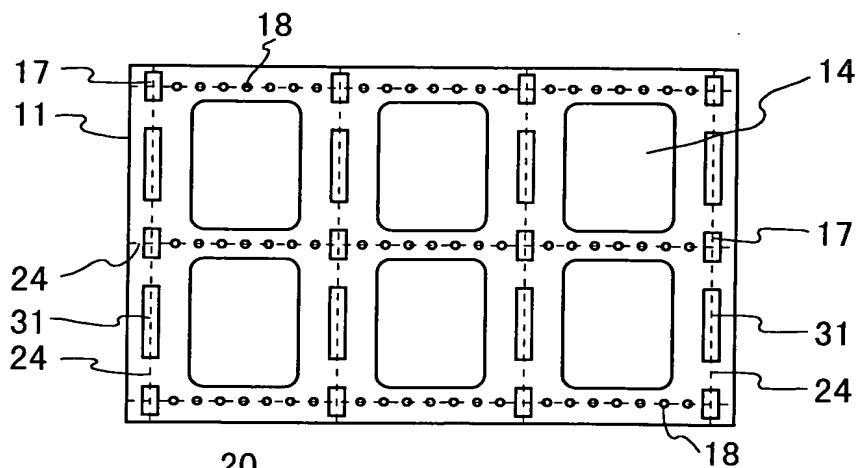


FIG. 1 B

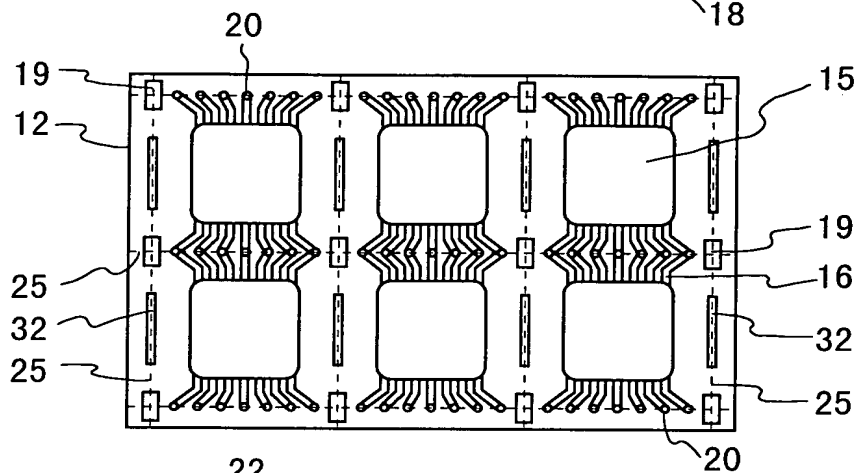
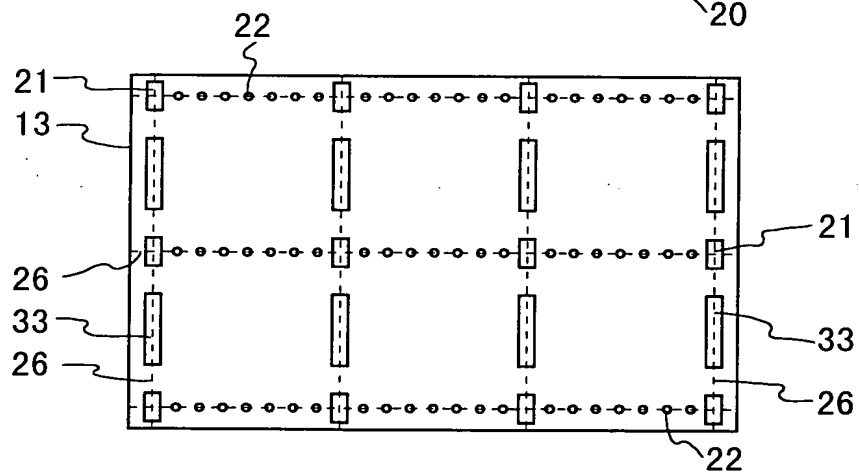


FIG. 1 C



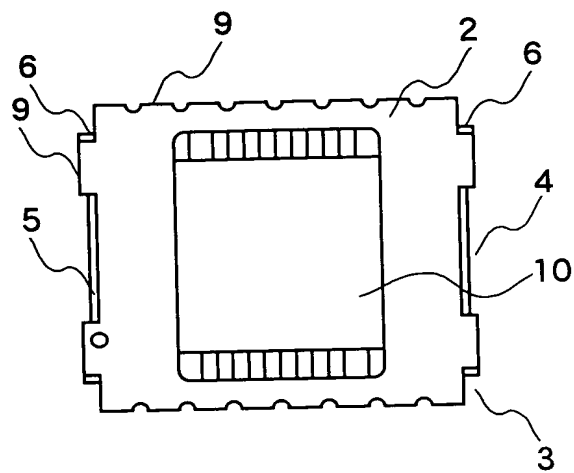


FIG. 2A

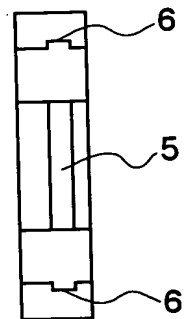


FIG. 2C

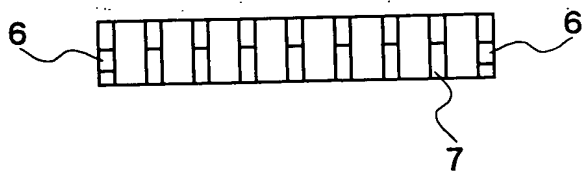


FIG. 2B

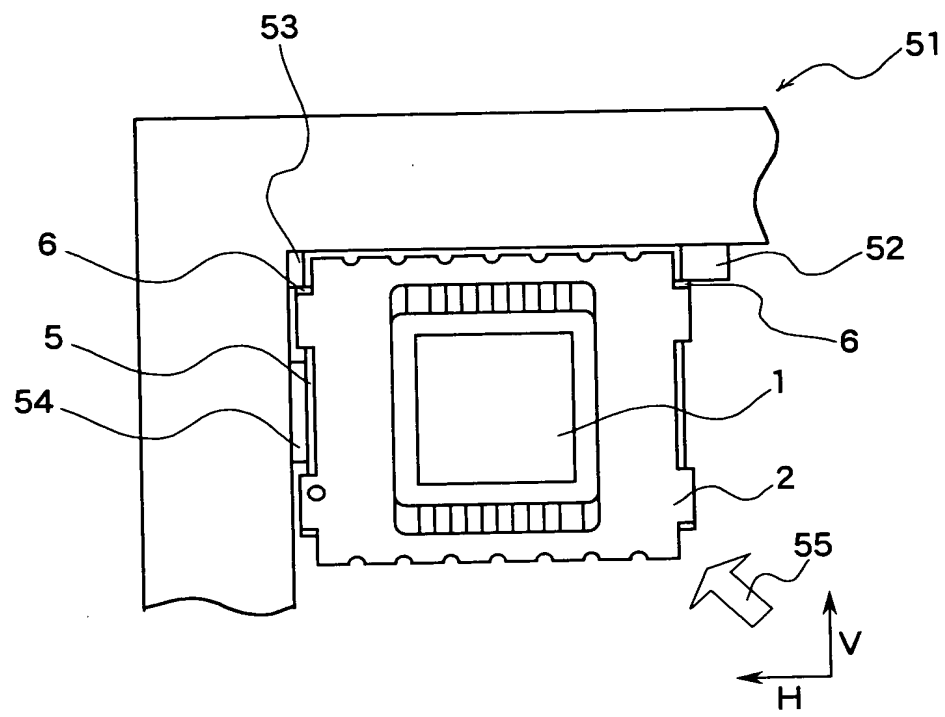


FIG. 3

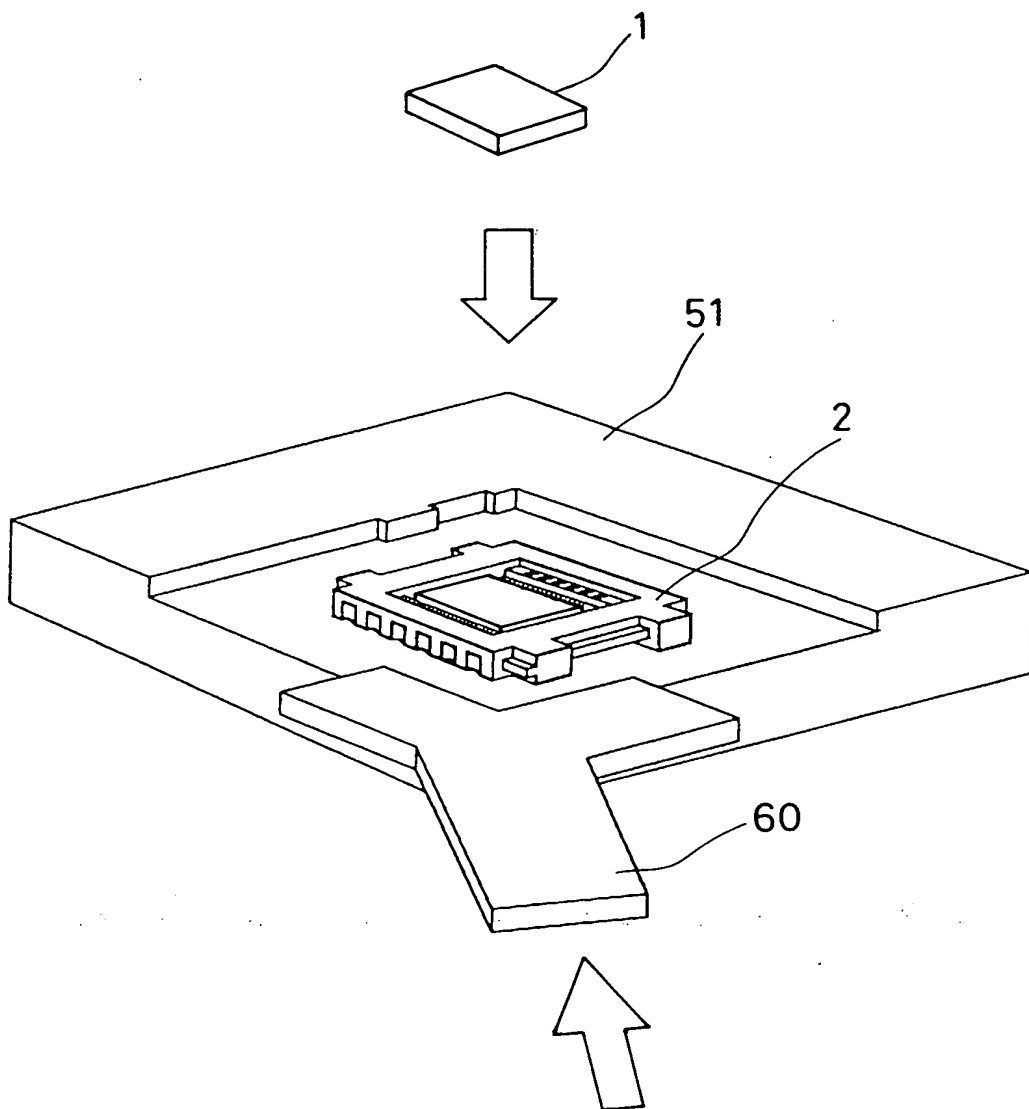


FIG . 4

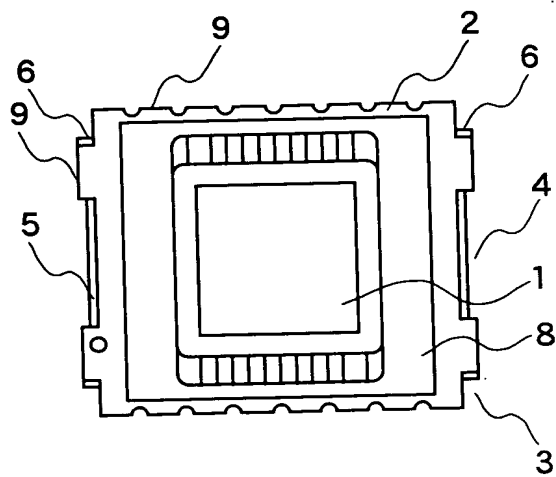


FIG. 5A

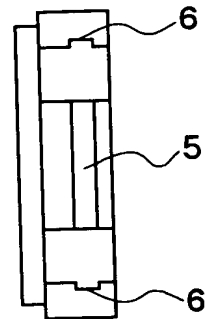


FIG. 5C

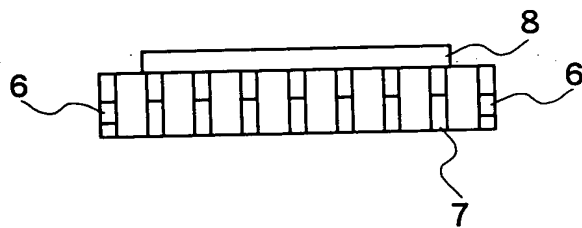


FIG. 5B

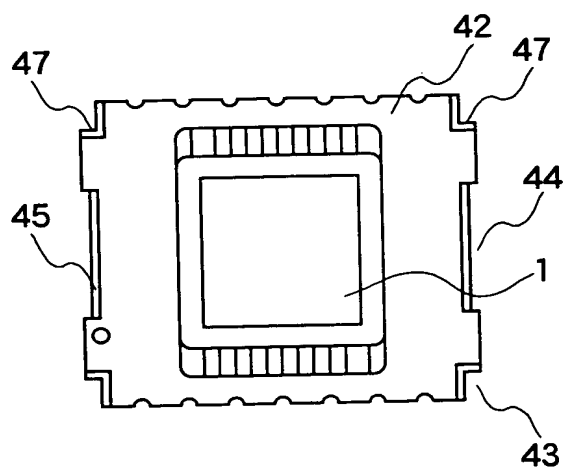


FIG. 6

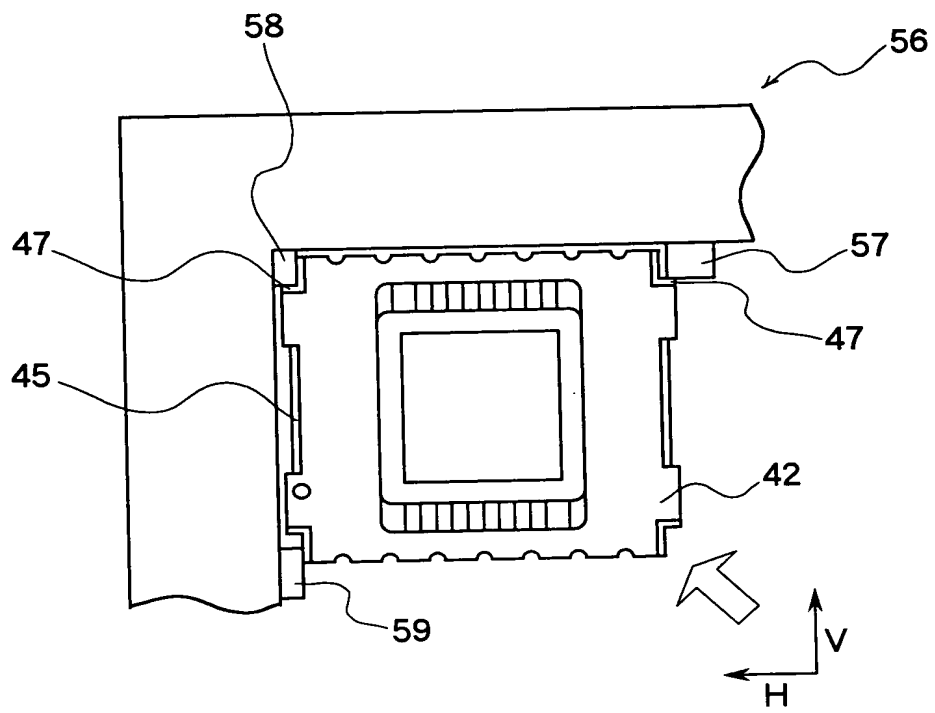


FIG. 7

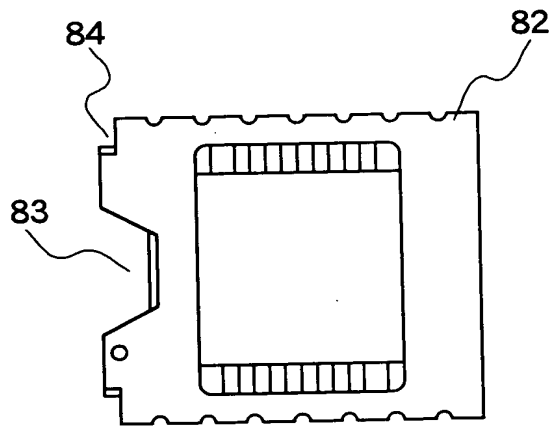


FIG. 8

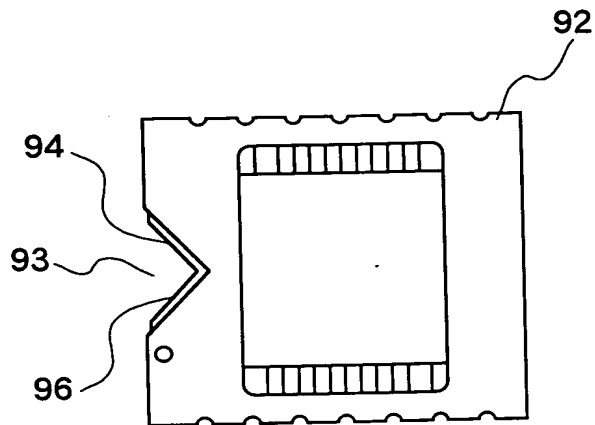


FIG. 9A

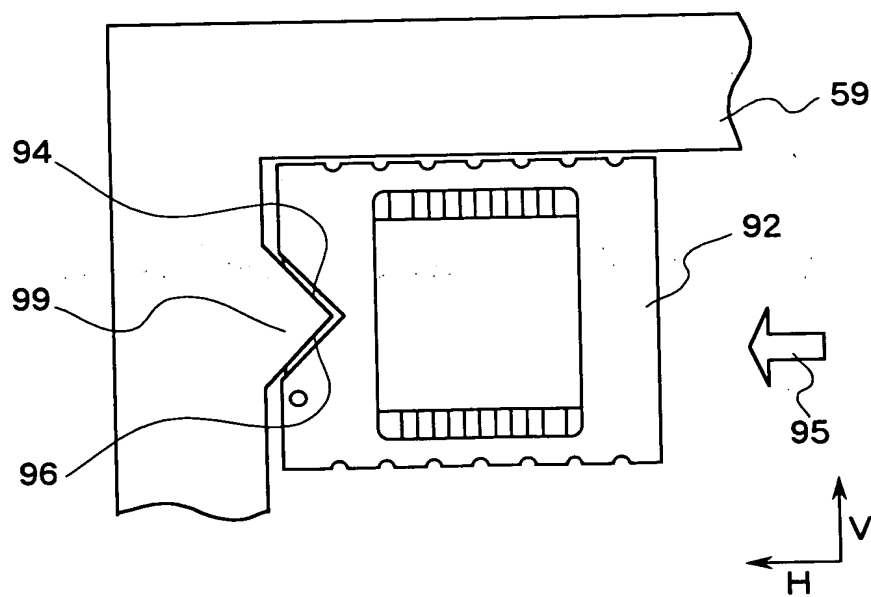


FIG. 9B

FIG. 10 is a perspective view of the device 100 in a disassembled state. The device 100 includes a base 61, a chip 62, and a substrate 63. The chip 62 is mounted on the substrate 63. The base 61 is positioned above the chip 62. The substrate 63 has a central circular feature 64. The chip 62 has a central square feature 65. The base 61 has a central circular feature 66. The device 100 is shown in a disassembled state, with the base 61, chip 62, and substrate 63 separated from each other.

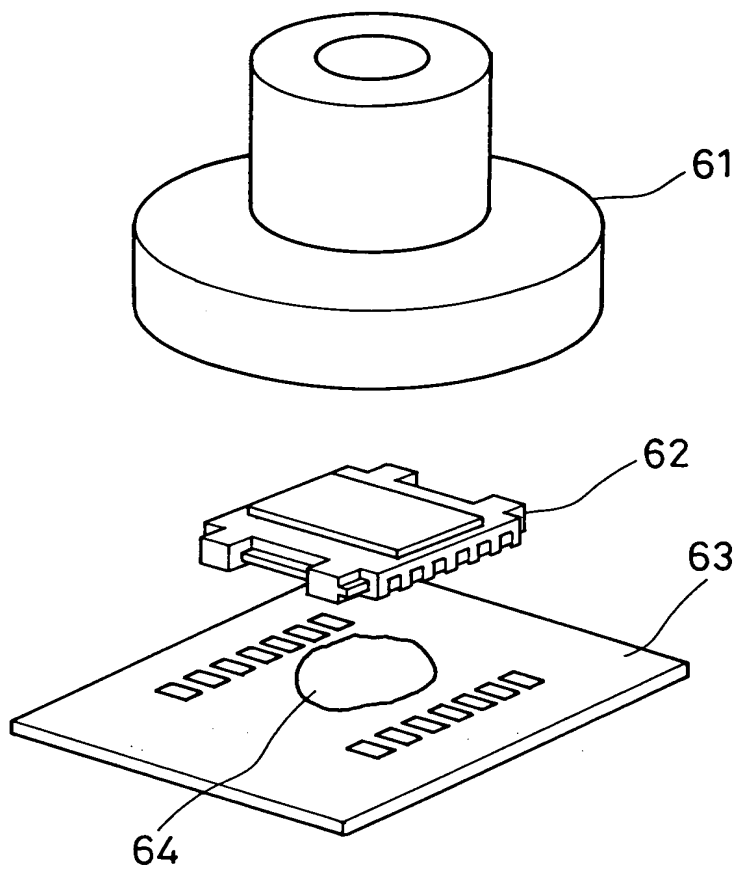


FIG . 10

FIG. 11 is a perspective view of the device 100 in a closed position. The device 100 includes a housing 60 and a cover 70. The housing 60 includes a base 61 and a side 62. The cover 70 includes a top 71 and a bottom 72. The device 100 is shown in a closed position, with the cover 70 covering the housing 60. The device 100 is shown in a perspective view, with the housing 60 and the cover 70 being the main components. The device 100 is shown in a closed position, with the cover 70 covering the housing 60. The device 100 is shown in a perspective view, with the housing 60 and the cover 70 being the main components.

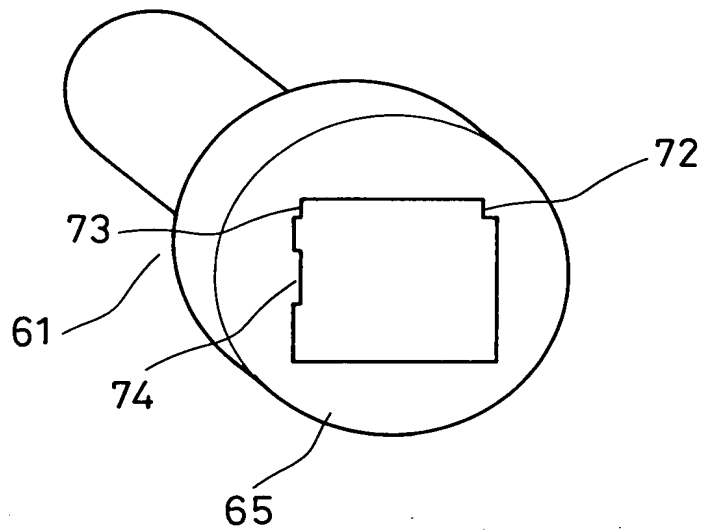


FIG . 11

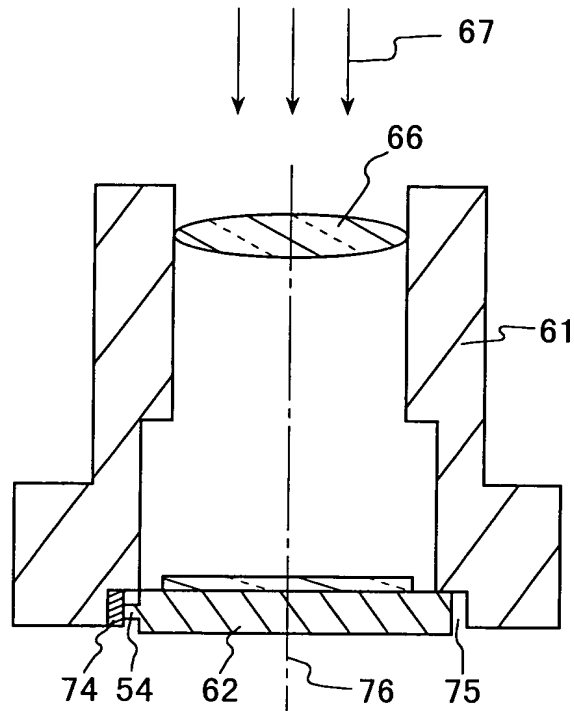


FIG. 12

FIG. 13 A

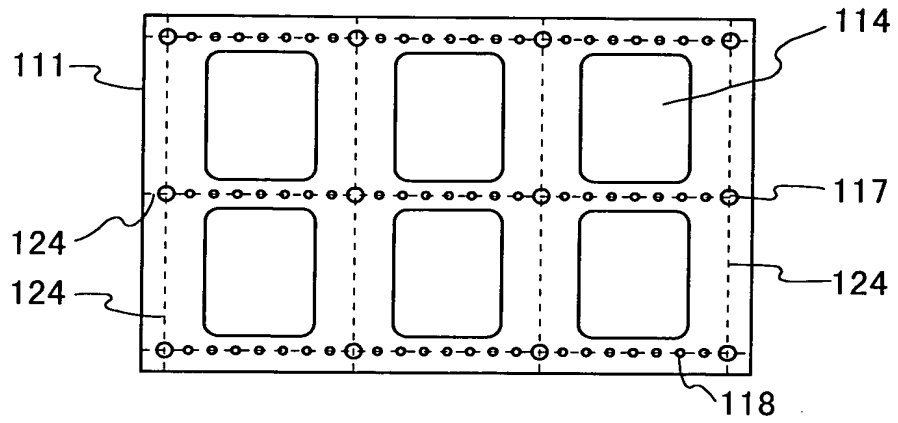


FIG. 13 B

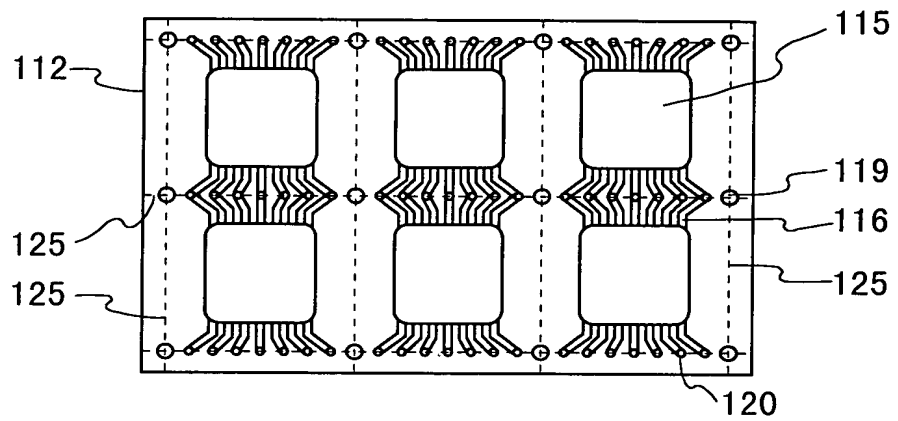
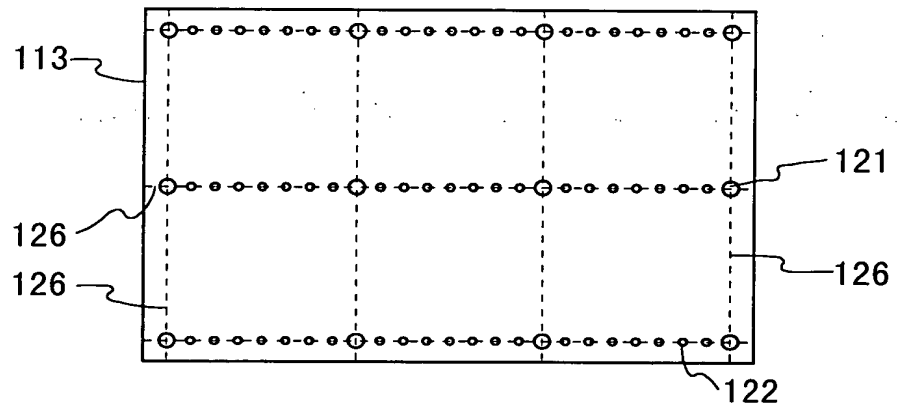


FIG. 13 C



PRIOR ART

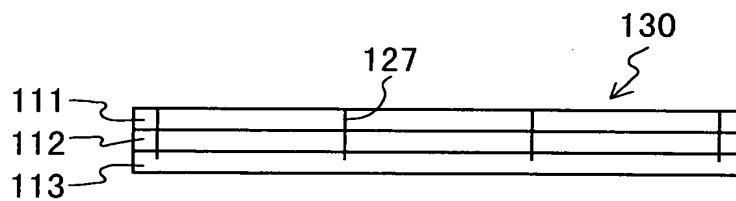


FIG. 14 (PRIOR ART)

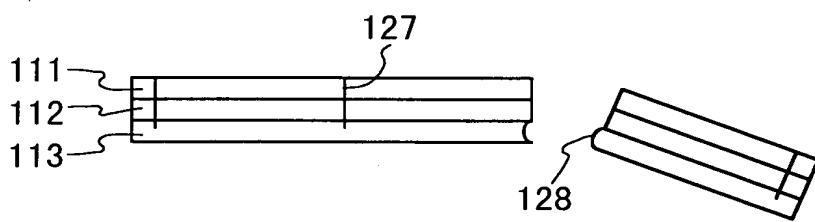


FIG. 15 (PRIOR ART)

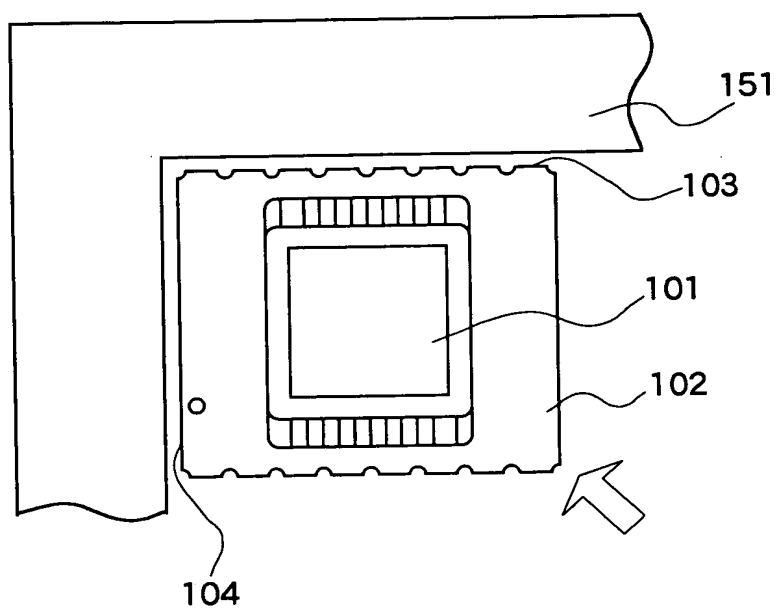


FIG. 16 (PRIOR ART)

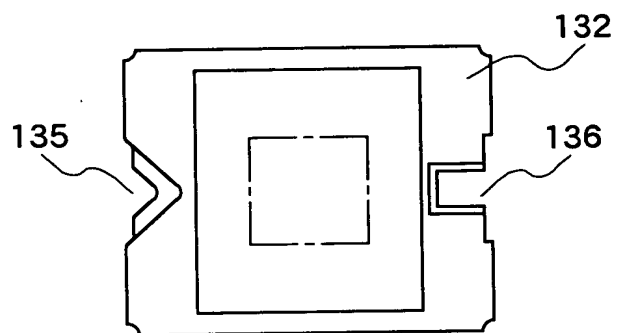


FIG. 17A (PRIOR ART)

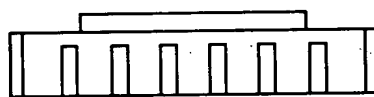


FIG. 17B (PRIOR ART)

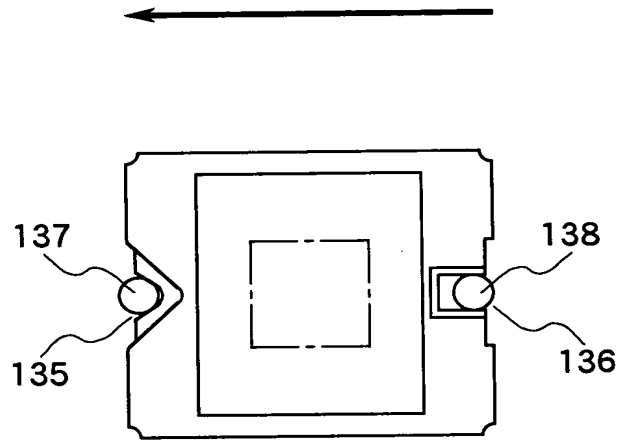


FIG. 18 (PRIOR ART)